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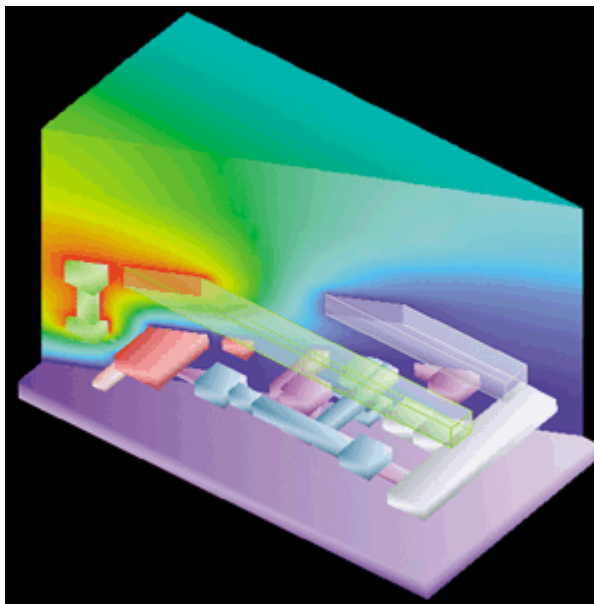
Raphael

Interconnect Analysis Software Product

Raphael is a collection of 2D and 3D field solvers and interfaces that provide the ability to obtain accurate interconnect models for different engineering needs. Given today's deep submicron process technologies, and increasing clock rates, interconnects fundamentally control the over: operating performance of high-speed systems. Interconnect structures must be fully and accur: characterized to ensure on-chip signal integrity. Raphael satisfies this critical industry need by rigorously simulating the resistance, inductance and capacitance with its industry-standard field solvers and interfaces.

RAPHAEL KEY FEATURES:

- Analyze complex on-chip interconnect structures and the influence of process variation.
- Create a parasitic database for both foundries and designers to study the effect of design rule change.
- Generate accurate capacitance rules for layout parameter extraction (LPE) tools.



RAPHAEL

Raphael is designed to simulate the electrical and thermal effects of today's complex on-chip interconnect. Through Raphael's easy-to-use graphical user interface (GUI), process technology data are entered and the critical interconnect structures are automatically generated and characterized for capacitance. Following thousands of automated field-solver simulations, Rapt gives the user the ability to conduct full regression analysis to create response surface models (RSM) representing interconnect parasitics.

```

Raphael: Output Terminal
File
Output

// Side-wall down component
CAPACITANCE CROSSOVER FRINGE MET. POLY INSIDE OF MET2 MASK
PROPERTY C
max_distance = 2.6
IF ( DISTANCE() > 0)
  C = 0.0552 * LENGTH() * (1.0 - EXP(0.3473 - 0.201 * DISTANCE()))
ELSE
  C = 0.0274 * LENGTH()
}
// Iter= 14, RMS Error= 0.1125%, Max Value= 0.02739
// Max Error= -0.05904%, at S= 1.2, Exact Value= 0.01735
// Side-wall up component
CAPACITANCE CROSSOVER FRINGE POLY MET1 INSIDE OF MET2 MASK
PROPERTY C
max_distance = 2.6
IF ( DISTANCE() > 0)
  C = 0.02073 * LENGTH() * (1.0 - EXP(0.139 - 1.236 * DISTANCE()))
ELSE
  C = 0.01983 * LENGTH()
}
// Iter= 11, RMS Error= 0.2473%, Max Value= 0.01983
// Max Error= 0.3774%, at S= 1.2, Exact Value= 0.0156

//-----
// NEARBODY CAPACITANCE
//-----

// STRUCTURE: POLY with BULK as a bottom ground plane.
CAPACITANCE NEARBODY POLY WITH SHIELD POLY MASK
PROPERTY C
max_distance = 1.2
max_width = 0.9
C = 0.194 * LENGTH() * (1.0 - 1.0 /
  (1.616 + 0.1657 * width1() + width2() * DISTANCE() ))
  * POW( ABS( DISTANCE() - 0.6661 ), -1.824 )
}
// Iter= 14, RMS Error= 0.2392%, Max Value= 0.04792
// Max Error= 0.6702%, at W= 0.8, S= 0.8, Exact Value= 0.03649

Close

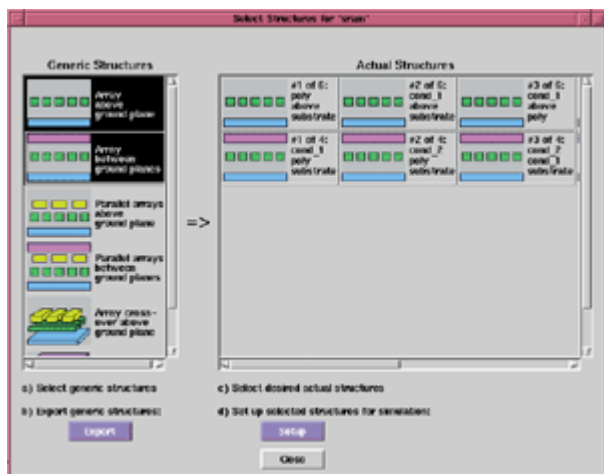
```

The LPE AAM generates capacitance rules for Mentor xCalibre.

Additionally, capabilities are provided for characterizing structures extracted directly from the layout simulated by Taurus-Topography, Avant!'s product for simulating etch and deposition. Raphael provides the link between process/device engineers and IC designers/layout engineers for understanding the implications of interconnect technology. Process and device engineers who use Raphael to establish process specifications and design rules when developing new technology, transfer parasitic information to designers via the Raphael Parasitic Database.

LPE AAM

The CAD engineer who supports interconnect parasitic extraction has the daunting task of providing accurate capacitance models for LPE tools. The LPE-AAM (Advanced Application Module) within Raphael automatically generates the capacitance models for such LPE tools as Mentor xCalibre and ICextract, and Cadence Dracula and Diva. The integration solution allows designers to obtain more accurate post-layout parameters for full chip and critical net analysis.



Critical structures are created automatically for field-solver simulations.

Raphael: Output Terminal

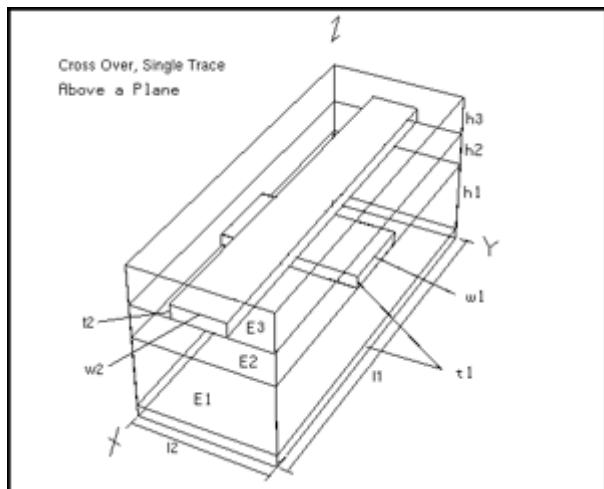
Generic Structure Name: Arr_nhnm_gp
Actual Structure Name: NET1, above, POLY

C Area: 3.453e-02

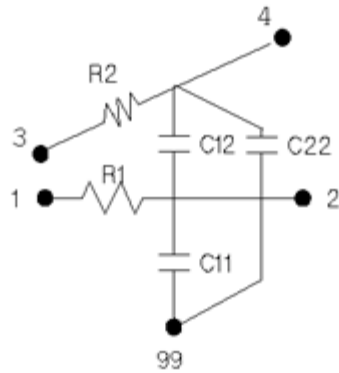
Width	Spacing	Cbottom	Ccoupli	Perimeter	Lateral
8.000e-01	5.000e-01	5.500e-02	7.919e-02	1.369e-02	4.751e-02
8.000e-01	3.000e-01	6.075e-02	6.226e-02	1.656e-02	4.981e-02
0.000e-01	1.000e+00	6.609e-02	5.151e-02	1.923e-02	5.151e-02
8.000e-01	1.200e+00	7.105e-02	4.401e-02	2.171e-02	5.281e-02
8.000e-01	1.400e+00	7.486e-02	3.720e-02	2.362e-02	5.208e-02
8.000e-01	1.600e+00	7.881e-02	3.273e-02	2.559e-02	5.237e-02
8.000e-01	1.800e+00	8.244e-02	2.914e-02	2.741e-02	5.245e-02
8.000e-01	2.000e+00	8.576e-02	2.619e-02	2.907e-02	5.238e-02
8.000e-01	2.200e+00	8.881e-02	2.372e-02	3.059e-02	5.218e-02
8.000e-01	2.400e+00	9.163e-02	2.162e-02	3.200e-02	5.188e-02
8.000e-01	2.600e+00	9.423e-02	1.980e-02	3.330e-02	5.149e-02
1.700e+00	3.000e-01	9.049e-02	6.790e-02	1.589e-02	5.432e-02
1.700e+00	1.000e+00	9.576e-02	5.669e-02	1.853e-02	5.669e-02
1.700e+00	1.200e+00	1.007e-01	4.881e-02	2.099e-02	5.857e-02
1.700e+00	1.400e+00	1.046e-01	4.172e-02	2.295e-02	5.841e-02
1.700e+00	1.600e+00	1.086e-01	3.696e-02	2.496e-02	5.914e-02
1.700e+00	1.800e+00	1.123e-01	3.311e-02	2.682e-02	5.960e-02
1.700e+00	2.000e+00	1.158e-01	2.993e-02	2.854e-02	5.986e-02
1.700e+00	2.200e+00	1.190e-01	2.724e-02	3.013e-02	5.993e-02
1.700e+00	2.400e+00	1.219e-01	2.494e-02	3.161e-02	5.987e-02
1.700e+00	2.600e+00	1.247e-01	2.295e-02	3.299e-02	5.967e-02
2.600e+00	5.000e-01	1.148e-01	8.952e-02	1.252e-02	5.371e-02
2.600e+00	3.000e-01	1.204e-01	7.168e-02	1.532e-02	5.735e-02
2.600e+00	1.000e+00	1.257e-01	6.020e-02	1.795e-02	6.020e-02
2.600e+00	1.200e+00	1.306e-01	5.207e-02	2.040e-02	6.249e-02
2.600e+00	1.400e+00	1.346e-01	4.481e-02	2.240e-02	6.273e-02
2.600e+00	1.600e+00	1.387e-01	3.986e-02	2.444e-02	6.378e-02
2.600e+00	1.800e+00	1.424e-01	3.500e-02	2.630e-02	6.453e-02
2.600e+00	2.000e+00	1.460e-01	3.251e-02	2.809e-02	6.503e-02
2.600e+00	2.200e+00	1.492e-01	2.969e-02	2.972e-02	6.531e-02
2.600e+00	2.400e+00	1.523e-01	2.726e-02	3.125e-02	6.543e-02
2.600e+00	2.600e+00	1.551e-01	2.515e-02	3.267e-02	6.538e-02

Close

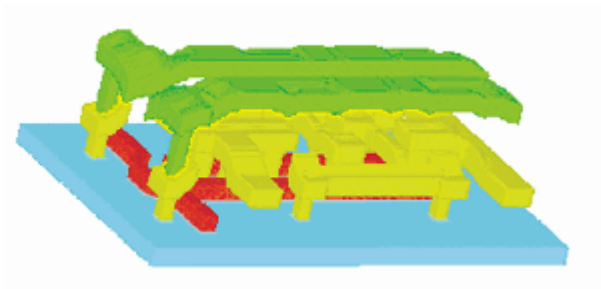
A capacitance table helps engineers study the effect of process or design rule change.



Two cross-over traces are only one of many structures that can be easily set up for simulation, entering only a few parameters.



A generated SPICE model for the cross-over structure



The Terrain interface lets Raphael users model realistic structures after etch and deposition.

RAPHAEL PARASITICS DATABASE

The Raphael Parasitics Database is the enabling environment for generating parasitic capacitance models. Raphael automatically characterizes the interconnect structures associated with different process technologies. With this capability, engineers can reduce the time required to set up and run simulations from several days or weeks to as little as a single day.

Using Raphael's GUI, engineers can easily generate capacitance tables and study the effect of process or design rule change. In addition, they can derive the regression equations through a built-in nonlinear optimization program.

COMPLEX ELECTRICAL AND THERMAL ANALYSIS

Raphael contains a collection of 2D and 3D Poisson field solvers to simulate resistance, inductance, capacitance, and potential, electric field, temperature, and current density distributions.

The Taurus-Topography interface enables Raphael to easily account for topography effects with an interconnect structure. Taurus-Topography is Avant!'s 2D and 3D deposition and etch simulator; the output of which can be directly read by Raphael to compute the resistance and capacitance of actual, instead of idealized, structures.

RAPHAEL INTERCONNECT LIBRARY AND SPICE MODEL GENERATION

With the Raphael Interconnect Library (RIL), you can easily set up, run and inspect a large number of different simulations. The library is composed of many typical geometries that represent common interconnect structures such as vias, pads and arrays of parallel traces. RIL allows the designer to perform many simulations by setting up a table of input values. A typical run not only produces lumped values for the resistance, capacitance and inductance, but also generates an associated lumped or distributed SPICE netlist.

SIMULATION FEATURES:

- Calculates capacitance, resistance, characteristic impedance, and potential, temperature and current density distributions.
- Simulates floating metals and anisotropic dielectrics.
- Solves Poisson's equation with automatic gridding.
- Computes 3D resistance and inductance with skin effect by quasi-magnetostatic approach.
- Finite difference method and boundary element method.

INTERFACES:

- IC layout GDSII files interface via Taurus-Layout for cell-level interconnect analysis.
- Taurus-Topography interface for post-fabrication simulation analysis.
- Avant! Star-RC, Mentor Graphics xCalibre and ICextract, Cadence Dracula and Diva interfaces for accurate full-chip post layout parameter extraction.

OUTPUTS:

- Lumped electrical elements for capacitance, resistance and inductance.
- SPICE equivalent circuit netlists for library structures.
- Distributions of potential, current density and temperature.
- RSM models from regression analysis.
- Capacitance rule files for LPE tools.

VISUALIZATION TOOLS:

- Taurus-Visual (1D, 2D and 3D graphics).
- DPLOT (2D and 3D graphics).

SYSTEM CONFIGURATION REQUIREMENTS:

- Platforms: Runs on UNIX workstations from DEC, Hewlett-Packard, IBM and Sun Microsystems.
- Memory: 64 MB.
- Disk Space: 120 MB.

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