A New Integrated Metal-Semiconductor Simulation Methodology for On-Chip Electrostatic Discharge Protection Design Optimization

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ABSTRACT

True design optimization of on-chip electrostatic discharge (ESD) protection structures is not yet possible using traditional simulation approaches, which focus on semiconductors only. This paper reports a new mixed-mode ESD simulation-design methodology with integrated metal-semiconductor simulation capability. The new approach can not only predict the design performance via coupled thermal-electro and device-circuit simulation, but also optimize the design by accurate sizing. The simulation results demonstrate that significant size reduction can be realized in ESD design using this new approach.

INTRODUCTION

Nowadays, on-chip Electrostatic Discharge protection design becomes a major challenge to IC designers as technology scaling moves into the very deep submicron (VDSM) regime. Since ESD structures normally consume large amount of chip area and inevitably produce parasitic capacitance, they may negatively influence performance of the circuits protected. Such ESD-induced parasitics become intolerant issues to high-speed and VDSM ICs and may affect such critical specifications as timing, stability, and bandwidth, etc.[1]. It is therefore desirable to optimize on-chip ESD protection design for both silicon structures and metal interconnects. The former can be addressed by traditional CAD work, while the latter is mainly guided by some empirical rules-of-thumb. For example, virtually all IC design rules suggest 20um of ESD metal line width or "better wide"[2]. The challenge is that there is no practical simulation approach that can simulate both semiconductors and metals altogether and simultaneously, leaving design of ESD metals largely with the experiences. This shortcoming certainly prohibits IC designers from optimizing ESD design, minimizing its impacts on circuits, and taking full advantages of some new technologies, *e.g.*, copper interconnects. This paper introduces a new simulation-design approach that intends to address such challenge.

SIMULATION PRINCIPLE

The new simulation approach was developed upon a novel predictive ESD simulation-design methodology with combined TCAD-ECAD simulation capability as described in [3]. Briefly, a proper ESD circuit model is used to generate the ESD pulses to stress the ESD unit under test and the ESD structure is simulated as a numerical device in ESD simulation. Mixed-mode device-circuit simulation is then performed to evaluate the ESD structure.

To conduct a complete metal-silicon simulation, metals are treated as semiconductor subjects by the numerical simulation tool, however, metal material parameters are used to substitute the silicon with the interconnects. In simulation, both metal and silicon are recognized as the simulation-able materials with different properties by the simulator. The mixed-mode ESD simulation is then performed for the whole structure to investigate the ESD protection circuits. The issues critical to successful simulation are parameter calibration and simulation convergence. The new simulation approach is illustrated in the following design example.

SIMULATION EXAMPLE

With the goal of providing a practical ESD design methodology, commercial CAD tool from Avant! Corp was used and a commonly used grounded-gate

NMOS (GGNMOS) ESD structure was selected as the test vehicle in this work. The design uses commercial 0.18µm six-metal aluminum and copper technologies from the UMC foundry service.

To better illustrate the new simulation approach, the overall work is discussed as a three-step simulation procedure for bare Si device, metal line, and complete ESD structure respectively. The schematics are illustrated in *Fig. 1* for human body model (HBM) ESD simulation.

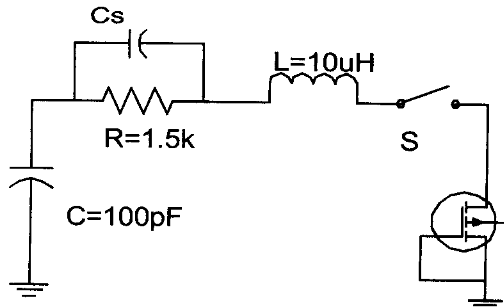

Fig. 1 HBM ESD simulation schematics

Part I: Bare Si Structure Simulation

Bare Si GGNMOS ESD protection devices, exclusive of metal interconnects, were simulated first to evaluate the Si structure itself. Two device sizes were chosen targeting 2KV and 4KV ESD protection, respectively. The simulated cross-section is shown in *Fig. 2*. The following critical dimensions were used according to the UMC ESD design rule: 0.33µm for channel length, 0.36µm for minimum *Source Contact to Gate Spacing* (SCGS), and 2.15µm for *Drain Contact to Gate Spacing* (DCGS).

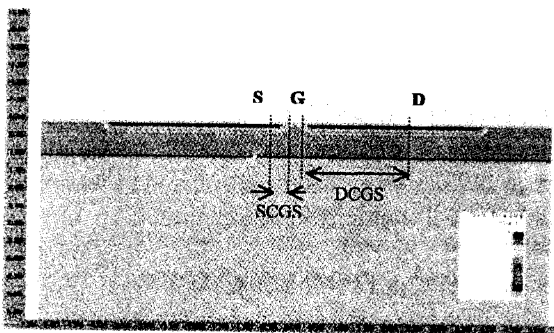

Fig. 2 A Cross-section for a bare Si device.

Both static and transient simulation[2] with devic circuit and electro-thermal coupling were the conducted for the devices. The criteria for ES damage used are material melting temperatur (1966°K for silicon), which are then compared wit the highest lattice temperature (T_{max}) in the silico device extracted from simulation. ESD failure i reported by the simulator when T_{max} exceeds $T_{melting}$. *Fig.3* shows how the ESD device was triggered o and driven into deep snapback during an ESD even *Fig. 4* shows ESD pulsing current and extracted T_m in time domain. *Fig. 5* shows the T_{max} ~ I curve. Th simulation data are summarized in *Table I*, with th following critical ESD parameters: triggering voltag (V_{t1}) of 4.7V, triggering time (t_1) of 0.08ns, an maximum sustainable current of 0.22A/µm for T_{max}= 1966°K. The simulation suggests that sizes of 56µ and 111µm are needed to survive 2kV and 4k ESDV stressing, respectively.

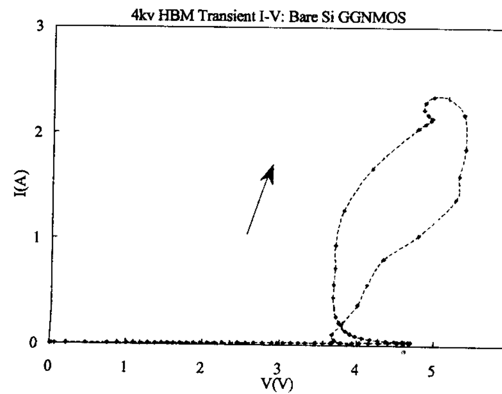

Fig.3 I-V curve during a HBM 4KV ESD test.

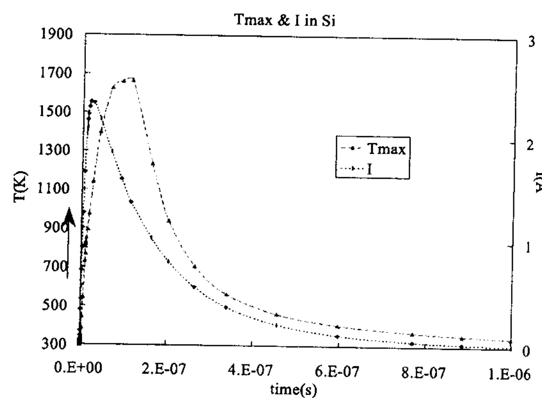

Fig.4 Transient T_{max} ~t & I~t curves under ESD.

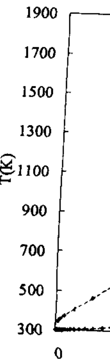

Fig.5 T_{max} ~

Table I ES

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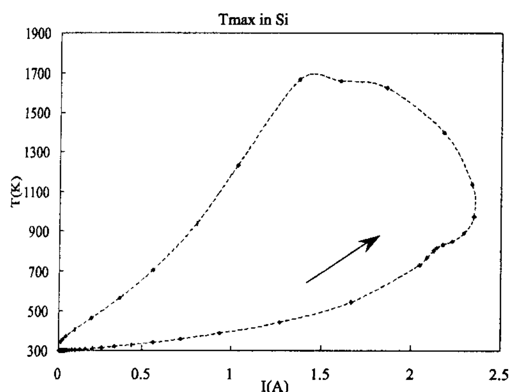

Fig.5 T_{max} ~ I curve during a HBM 4KV ESD test.

Table I ESD simulation data for bare Si devices

ESDV	2KV	4KV
V_{t1} (V)	4.70	4.70
t_1 (nS)	0.080	0.079
Min. pass-width (μm)	56	111
Sustainable I-density (A/μm-W)	0.022	0.023

Part II: Individual ESD Metal Line Simulatio

Individual metal line ESD simulation was then performed to investigate how the metal line itself behaves during ESD events. Stand-alone metal lines sandwiched between different interlayer dielectrics (ILD), to mimic the real-world situation, were simulated for this purpose. A simulated metal line structure example (20μm long and 0.3μm thick) is shown in *Fig.6*. The critical material parameters[4,5] used in simulation are listed in *Table II*.

Table II Critical parameters for ESD simulation

Material parameters	Al	Cu	Si
Melting -Temp. (°K)	933	1357	1966
Density, ρ (Kg/cm³, x 10⁻³)	2.7	8.96	2.32
Specific heat, C_p (J/Kg-°C)	899.6	385	850.9
Thermal resistivity κ (W/°C-cm)	2.212	4.01	33.3
Resistivity, ρ (μΩ-cm)	3	2.7	--

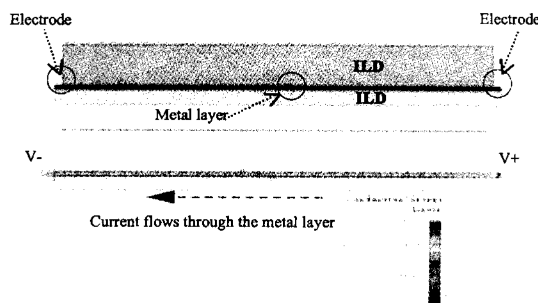

Fig.6 A single metal line sandwich structure used for ESD simulation of pure metal lines (upper). Simulation shows current flowing through the metal line in ESD test as expected (lower).

ESD simulation for both Cu and Al metal lines were performed under 2kV and 4kV ESD stressing by applying the ESD pulses across its two opposite electrodes. The maximum lattice temperature, T_{max}, was then extracted and compared with the $T_{melting}$ to decide whether the metal lines pass or fail the ESD tests. *Fig. 6* clearly shows the current flow in the metal line only, as expected. A pair of typical I~V and T_{max}~I curves are shown in *Fig.7* for an Al simulation under 4KV. Both ohmic I~V behavior and self-heating were observed for the metal line, indicating self Joule heating indeed occurs within metals that cannot be observed in traditional simulation. The important observations from the simulation are the following. (1) The width of metal line needed is much narrower than the commonly used 20μm for 2kV, indicating over-conservative existing design rules. (2) For the same ESD protection level, copper interconnects are more ESD robust compared to Al, resulting in an increase in maximum sustainable current density (~30%) and reduction in width (~30%). Therefore, much narrower metals may be expected for ESD design in using Cu interconnects than using Al, hence leading to less ESD parasitics. The simulation results are summarized in. *Table III*.

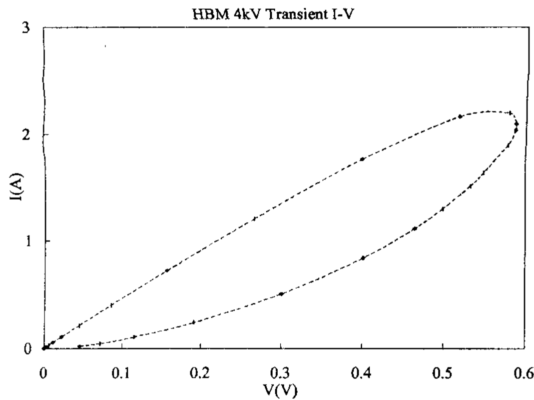

Fig.7a I-V characteristics of a single Al metalline under 4KV transient ESD test.

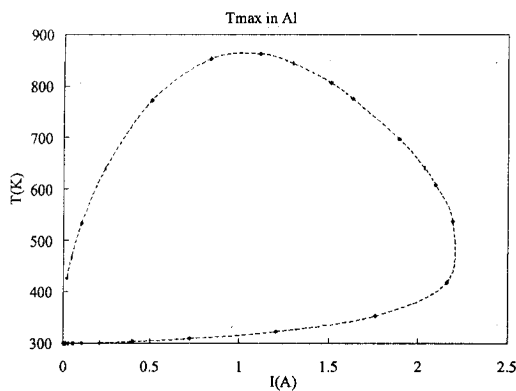

Fig.7b T_{max} ~ I curve during a HBM 4KV ESD test.

Table III Metal width needed & sustainable I-density

Item	ESD	Cu	Al
Metal line width (μm)	2kV	5	7
	4kV	10	15
Current density ($A/\mu m^2$)	2kV	0.636	0.488
	4kV	0.636	0.418

Part III. Simulatiomf Si + metal line

Finally, complete ESD protection structures including both metal lines and Si structure underneath were simulated to study performance of a real-world ESD protection unit as a whole.

A complete GGNMOS ESD structure is shown in *Fig. 8*. During ESD simulation, T_{max} data for both silicon and metals were extracted and compared with *the corresponding* $T_{melting}$. Whichever reaches the melting point first causes the device failure. An example simulated temperature contour is also shown in *Fig. 8*, which clearly demonstrate the self-heating occurs both in silicon near the drain channel and in metals. Therefore, this new ESD simulation approach provides the insights for IC designers to optimize ESD design in a whole scale, hence realizing an optimized design for both better ESD robustness and less parasitic effects.

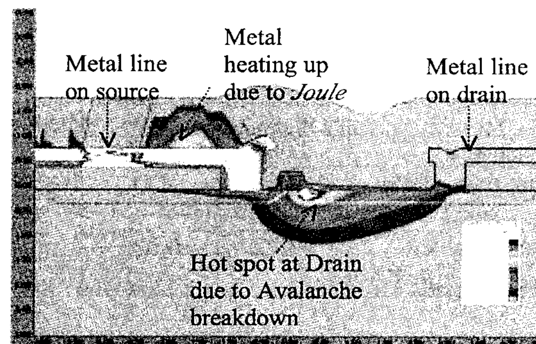

Fig.8 Simulated T-contour image shows thermal defects in the metal layer as well as in the Si channel.

SUMMARY

In conclusion, a new mixed-mode ESD simulation-design methodology with integrated metal-semiconductor simulation capability was developed. The simulation results demonstrate that significant size reduction can be realized in ESD design using this new approach. The new method can therefore be used in practical ESD design to ensure both better ESD robustness and less parasitic effects.

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