A COMPARISON STUDY OF ESD PROTECTION FOR RFIC'S: PERFORMANCE *vs.* PARASITICS

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Abstract

This paper reports two advanced Electro-Static Discharging (ESD) protection structures suitable for RFIC's and a comparison study of influences of ESD parasitic capacitance (C_{ESD}) on high-speed circuits. For a 4 Ghz ring-oscillator and a low-power high-speed Op-Amp circuits, it was observed that C_{ESD} may corrupt high-speed performance significantly and new ESD structures can recover the corruption by 80%.

Introduction

On-chip *ESD* protection design becomes a major challenge in high frequency and very deep sub-micron (*VDSM*) IC design due to Si consumption and parasitic effects. For example, advanced RF IC chips require not only high ESD failure threshold voltage (ESDV>4KV), but also low parasitic capacitance and resistance that exist in all ESD units. Parasitic ESD capacitance (C_{ESD}) is normally ignored in designs. However, in high frequency design, *e.g.*, RFIC's, C_{ESD} may be a killing factor. Traditional MOS-based ESD protection structures are not suitable to RFIC's because of its large size, hence high C_{ESD}. It is imperative to develop novel ESD protection devices for high-speed applications.

A complete full-chip ESD protection scheme is illustrated in *Fig. 1*, in which each bond-pad requires proper ESD protection devices. The ESD structures should be able to protect the chip against all ESD pulsing modes, *i.e.*, I/O-to-V_{DD} positively (*PD*) and negatively (*ND*) by ESD 1 & 3, I/O-to-ground (GND) positively (*PS*) and negatively (*NS*) by ESD 2 & 4, and from V_{DD}-to-GND (DS) by ESD5[1] . In multi-supplies cases, ESD devices are also required between power buses (ESD 6 & 7). Clearly, if large ESD devices are used, one may encounter significant parasitic C_{ESD}, especially in high-pin-count design. In this paper, two compact ESD structures are reported. A comparison study of using conventional MOS ESD protection structures and the two new ESD designs will be discussed on the impacts of C_{ESD} on circuit performance. The sample circuits used in this study are a GHz ring-oscillator clock generator and a low-power, high-speed Op Amps circuits.

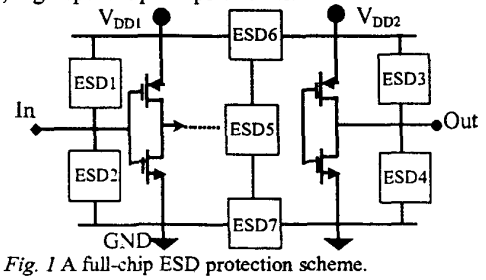

Fig. 1 A full-chip ESD protection scheme.

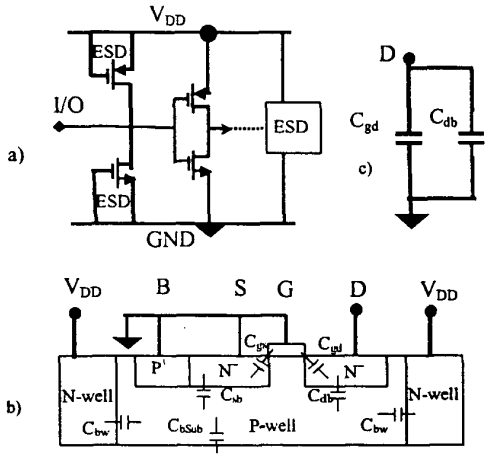

Fig. 2 ESD*a*: a) schematics, b) X-section, & c) C_{ESD} model.

ESD Design and Measurements

This work compares the conventional CMOS ESD structure (ESD*a*) with two new novel ESD structures (ESD*b* & ESD*c*)[2, 3] under the same ESDV = 4KV. The design was guided by an in-house developed mixed-mode ESD design-simulation methodology [4] for design prediction.

A. ESDa: MOS ESD structures

Fig. 2 illustrates the conventional MOS ESD protection structure. Normally, ground-gate NMOS and PMOS devices (GGNMOS & GGPMOS) are used to protect against ESD stresses at I/O pins *w.r.t* V_{DD} and GND (PD. ND, PS, & NS)

Table I Data for ESD performance from simulation & measurement

ESD devices	Methods	Triggering V_{t1} (V)	Holding V_h (V)	R_{ON} (Ω)
ESD *a*	Simulation	14.68	6.92	~1.9
	C-tracer	12.56	6.48	-
	TLP	12.5	6.5	~1.02
ESD *b*	Simulation	23.32	1.58	0.73
	C-tracer	22.8	1.55	-
	TLP	21.75	2.96	1.4
ESD c	Simulation	20.82	1.31	0.5
	C-tracer	22.5	1.5	-
	TLP	21.66	2.41	1.37

	ESD pass level		Simulated ESD device triggering time t_1 (nS)
	Simulation	HBM Test	
ESDa,200μ	4KV	4KV	0.2
ESDb,50μ	4KV	4KV	0.18
ESDc,50μ	4KV	4KV	0.16

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as shown in *Fig.2a*. An extra ESD unit is needed for V_{DD}-to-GND protection. *Fig. 2b* is a typical NMOS cross-section that shows parasitic junction capacitance. Because the gates are grounded, only C_{gd} and C_{db} have effects as modeled by *Fig. 2c*. Both NMOS and PMOS ESD structures contribute to the overall parasitic capacitance, C_{ESD}. Multiple-finger MOS structure is used as usual. From ESD simulation, four 50μm-long NMOS fingers were needed to achieve ESDV of 4KV design goal. ESD measurements include quasi-DC tests by curve tracer (Tektronik 310), transient tests by a transmission-line-pulsing tester (Barth 4002), and standard HBM zapping tests (IMCS 10000). The ESD structure passed 4KV HBM stressing as designed. ESD data from simulation and measurements shows good match as shown in *Table I*. The extracted C_{ESD} data are listed in *Table II*.

Table II C_{ESD} data (exclusive V_{DD}-Gnd protection)

For same ESDV=4KV		ESDa	ESDb	ESDc
Parasitic	Half ESD,1x	0.27	0.044	0.07
C_{ESD} (pF)	Full ESD,2x	0.54	0.09	0.07

B. ESDb: A Dual-Direction ESD Structure

Ideally, an ESD protection unit should provide low-impedance current shunting-channels formed by *active* devices in all ESD stressing modes (PD, ND, PS & NS). However, in the NMOS ESD structure, only one current discharging path is formed by a NPN device, with a reverse-biased parasitic diode serving as 1-shunting path in the opposite direction. There are two shortcomings: first, the reverse-biased diode has high impedance that limits the ESDV level; second, it can not be used for V_{DD}>5V because 10% ΔV_{DD} may turn on the diode accidentally. A new dual-direction ESD protection structure (ESDb) was designed to address this problem as illustrated in *Fig. 3*. Briefly, ESDb is a two-terminal (A & K), five-layer ($N_1P_2N_3P_4N_5$) structure consists of one lateral PNP transistor (Q_1=$P_2N_3P_4$), two vertical NPN transistors (Q_2=$N_1P_2N_3$ & Q_3=$N_3P_4N_5$) and four parasitic resistors, R_1, R_2, R_3, & R_4. The structure is connected to form two functional SCR units: unit 1= Q_1, Q_2, R_1 & R_3 and unit 2= Q_1, Q_3, R_2 & R_4 with *A* and *K* being the electrodes. In operation, when a positive ESD pulse appears at *A* (*w.r.t. K*), *BC* junction (N_3P_4) of Q_1 is reverse biased to its breakdown and the generated holes are collected by the negative terminal *K* via P_4-P^+ layer. Since both the P_4-P^+ and N_5-N^+ layers are connected to *K*, V_{BE} (P_4N_5) of Q_3 increases and eventually turns on Q_3. The SCR unit 1 ($P_2N_3P_4N_5$) is therefore triggered off (at V_{t1}) and driven into deep snapback region (holding voltage $V_h \leq 2V$). An *active* discharge path with negligible impedance R_{ON} is thereby formed to shunt the huge current surge and clamp the I/O pad voltage at a sufficient low level ($V_h \leq 2V$), thus protects *IC*s from being ESD-damaged. After the ESD pulse is over, the thyristor is quickly discharged and then turned off when the current decreases to below its holding current level. Similarly, the SCR unit 2 ($P_4N_3P_2N_1$) operates during a negative ESD pulse event (*K w.r.t. A*). Hence this forms a

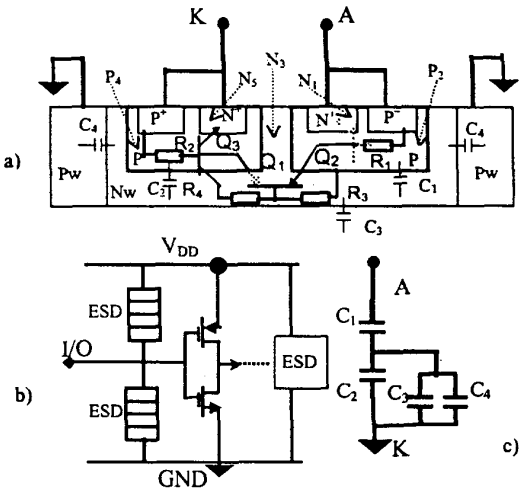

Fig. 3 ESD*b*: a new dual-direction ESD protection device.

dual-direction ESD protection device. Symmetric operation is illustrated in *Fig. 4*. ESD data from simulation and measurements are listed in *Table I*. A 50μm device passed HBM ESDV=4KV as designed and a 200μm device passed 14KV (test limit). Compared to the MOS ESDa, the ESDb features dual-polarity operation and small size. Therefore, ESDb has much lower C_{ESD} as shown in *Table II*, which greatly reduces the capacitive effects on the circuits. However, two ESDb's are still needed for each I/O pin for I/O-to-V_{DD} and I/O-to-Gnd, respectively. In addition, one extra ESD protection unit is needed for V_{DD}-to-Gnd protection as is in the MOS ESD case. Hence sizable C_{ESD} still exists, especially in high-pin-count cases.

C. ESDc: An All-Direction ESD Structure

To improve ESDb, a new all-direction ESD protection

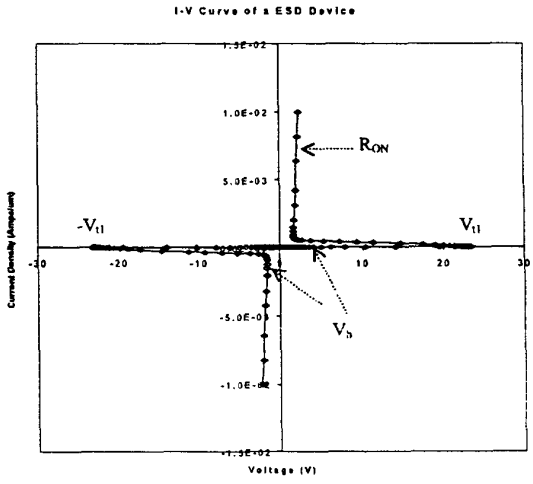

Fig. 4 Simulated I-V curve of ESD*b* shows symmetry.

structure (ESDc) was designed. ESDc is a three-terminal (*A, K_1, & K_2*) device with eight layers (*N_1, P_2, N_3, P_4, N_5, N_6, P_7, N_8*) as illustrated in *Fig. 5a*. It consists of six bipolar transistors and eight parasitic resistors, which are electrically connected to form two ESDb-type functional units. Unit I consists of Q_1= $P_2N_3P_4$, Q_2=$N_1P_2N_3$, Q_3=$N_3P_4N_5$, R_1, R_2, R_3 & R_4. Unit II has Q_4= $P_4N_3P_7$, Q_5=$N_6P_4N_3$, Q_6=$N_3P_7N_8$, R_5, R_6, R_7 & R_8. Q_3 and Q_5 share base and collector layers. R_2 and R_5 split the resistor of layer P_4. A complete full-ESD protection scheme using ESDc is shown in *Fig. 5b*. Operation of ESDc is basically a dual-operation of ESDb units. Its three electrodes, A, K_1 & K_2, are connected to I/O pin, V_{DD} and Gnd, respectively, on a chip. It is normally off. During ESD events, when ESD pulses appear at I/O pin *w.r.t.* to V_{DD} or GND, the Unit I or Unit II will function exactly the same way as the ESDb device does to provide adequate ESD protection correspondingly as described in Section B. ESDc also operates symmetrically as shown by one measured I-V curve in *Fig. 6*. Typical ESD data from simulation and tests are listed in *Table I*. To achieve 4KV design goal, a 50μm device was needed, while a 200μm device passed over 14KV HBM stressing. The major advantages of the ESDc over the ESDb are the following. First, *one* ESDc device for each I/O pin can provide ESD protection against all four ESD pulsing modes: ND by path ①, PD by path ②, PS by path ③, and NS by path ④ as shown in *Fig. 5b*. Second, a similar ESDb-type SCR device exists between terminals K_1 and K_2, which forms a discharging path ⑤ to protect ESD surge from V_{DD} to GND (DS). Therefore, one single ESDc-type device is enough to provide complete ESD protection for each I/O, including power buses. Third, it hence introduces much lower parasitic C_{ESD} as shown in *Table II*. Another advantage of ESDc is that it is suitable for bondpad-oriented ESD design and is layout friendly. Overall, ESDb represents ~83% reduction in C_{ESD} compared to CMOS ESDa, while ESDc further reduces C_{ESD} by ~ 22% over ESDb, therefore benefit circuits.

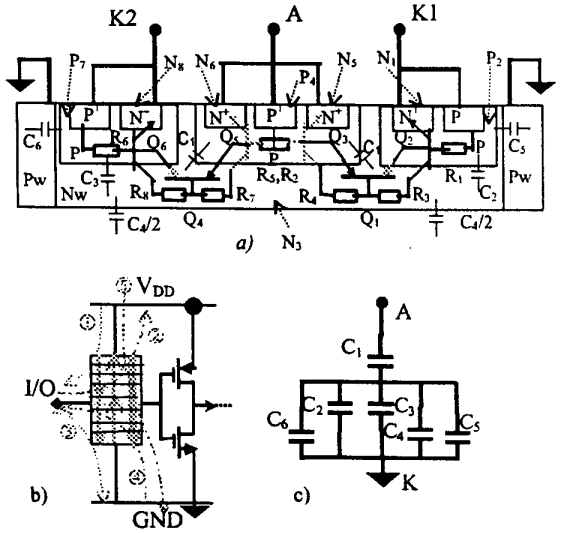

Fig. 5 ESDc: a)X-section; *b)* schematics & *c)* C_{ESD} model.

Influences of C_{ESD} on High-Speed Circuits

Two circuits were designed to demonstrate the merits of the new ESD structures to high-frequency IC designs: a GHz ring-oscillator and a low-power, high-speed Op-Amp, using a 0.18μm 1.5V commercial CMOS technology.

A. Improvement in Ring-Oscillator Clock Frequency

To demonstrate how seriously C_{ESD} of ESD*a* units may degrade IC speed and how the new ESD structures, ESD*b* & ESD*c*, can alleviate this problem, a ring-oscillator circuit normally used to generate on-chip clock signals is designed. 15 stages were chosen for measurement concern and the targeting clock frequency was 4 Ghz. Since overall C_{ESD} effect in practical circuits varies according to I/O pin counts, two ESD loading situations were considered in this work: a single-load scenario representing the least effect where only one I/O pin has ESD unit and a full-load scenario showing multi-pin ESD connection where ESD units were connected to each stage. Simulated signal waveforms are shown in *Fig. 7* with delay time and frequency data listed in *Tables III & IV*. It is observed that C_{ESD} of ESD*a* dramatically reduced the clock speed by 85% to 99% for single-load and full-load cases, respectively. However, the new ESD structures can recover the corruption significantly, 41% for ESDb and 62% for ESDc, respectively, in the single-load case.

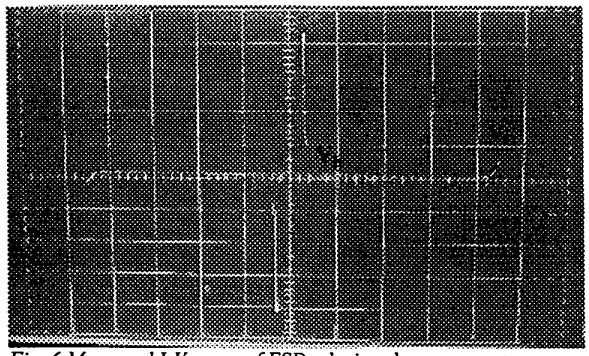

Fig. 6 Measured I-V curve of ESDc device shows symmetry.

Table III Influences of C_{ESD} on a 15-stage ring-oscillator circuit

ESD type	Cap-load	C_{ESD} (*p*F)	t_d (nS)	*f* (MHz)
None	Original	0	0.211	4739
ESDa	Single load: 1xC_{ESD}	0.54	1.343	744.6
ESDb		0.09	0.416	2402
ESDc		0.07	0.31	3226
ESDa	Full load: 15xC_{ESD}	0.54	23.91	41.82
ESDb		0.09	4.106	243.5
ESDc		0.07	3.291	303.9

Table IV Speed degradation *w.r.t.* original clock freq. due to C_{ESD}

ESD load	Original	ESDa	ESDb	ESDc
Single ESD load	0	-84.92%	-49.31%	-31.92%
	Improve-ment	⬌ +41.50% ⇃		
		⬌ -62.13%	⇃	

B. Improvement in Hi-Speed Op-Amp Performance

A low-power, high-speed, wide-swing Op Amp circuit, designed for wireless communication applications, was used

to demonstrate the influences of parasitic C_{ESD} on overall performance of a functional chip. The circuit topology, as shown in *Fig. 8*, features differential input, push-pull output stage for wide swing, level shift, capacitive compensation with nulling resistor for better stability, and global biasing for low-power. The critical performance data are listed in *Table V* that shows very low power consumption of 0.4 mW, high unity-gain and -3dB band-width of 126MHz and 40 KHz, wide swing of 0.96V measured at 80% small-signal gain, very high slew-rate of 115 mV/nS, and short settling time of 9 nS measured at 1% of the output.

Table V Op Amp critical specifications (C_L = 1 pF)

Technology	0.18um, 1.5V	Power supply (V)	1.5
Gain (dB)	74.16	Power cons. (mW)	0.41
Phase margin	61.3°	V-swing (V, 80%)	0.964
f_T (MHz)	126.3	f_{3dB} (KHz)	40.6
SR (mV/nS)	115.7	Settling time (ns, 1%)	9.38

To evaluate the negative impacts of ESD on the Op Amp performance, C_{ESD} were connected to the output node for ESDa, ESDb and ESDc, respectively. *Fig. 9* shows a sample small-signal step response for settling time measurements. The typical data are summarized in *Table VI & VII*. It is clear that the traditional CMOS ESD protection devices (ESDa) can substantially deteriorate performance of the high-speed Op Amp, *i.e.*, over 30% deterioration in unity-gain band-width, slew rate and settling time, all of which are critical in high-speed operation. Using the two advanced ESD structures (ESDb & c), the performance corruption may be recovered by 60 ~ 80% in this case.

Although this comparison study used two example circuits only, It is interesting to observe that, while higher ESD specifications is in demand, parasitic effects from the ESD protection units used may dramatically affect the core circuit being protected. Advanced low-parasitic ESD structures are important in RFIC designs and a designer must pay special attention to ESD side effects in high-speed designs.

Table VI Influences of C_{ESD} loads on an Op Amp at C_L = 1pF

ESD	C_{ESD}(pF)	f_T(MHz)	f_{3dB}(KHz)	SR(mV/ns)	t_{set}(nS)
None	0	126.3	40.6	115.7	9.38
ESDa	0.54	86.2	37.6	80.6	13.09
ESDb	0.09	112.2	39.8	107.6	10.28
ESDc	0.07	118.6	39.8	109.3	10.13

Table VII Op Amp performance degradation due to C_{ESD} loads

Parameters	Original	ESDa	ESDb	ESDc
f_T (MHz)	126.3	-31.75%	-11.16%	-6.1%
		⬎ +64.85% ⬆		
		⬎ +80.86%		⬆
f_{3dB} (KHz)	40.6	-7.4%	-2%	-2%
		⬎ +83.78% ⬆		
		⬎ +83.78%		⬆
Slew rate (V/us)	115.7	-30.34%	-7%	-5.5%
		⬎ +76.93% ⬆		
		⬎ +81.87%		⬆
t_{set} (nS, 1%)	9.38	-39.55%	-9.59%	-8%
		⬎ +75.98% ⬆		
		⬎ +79.77%		⬆

Conclusions

In summary, a pair of novel, low-parasitic ESD protection structures for RFIC's was described. A comprehensive comparison study of possible ESD side-effects on the high-speed circuits protected was discussed. It was observed that ESD induced parasitic effects may degrade circuit performance significantly, while advanced low-parasitic ESD structures could substantially recover this type of circuit performance corruption. It is therefore imperative to use low-parasitic ESD protection and to include ESD related parasitic effects in RF and VDSM IC designs.

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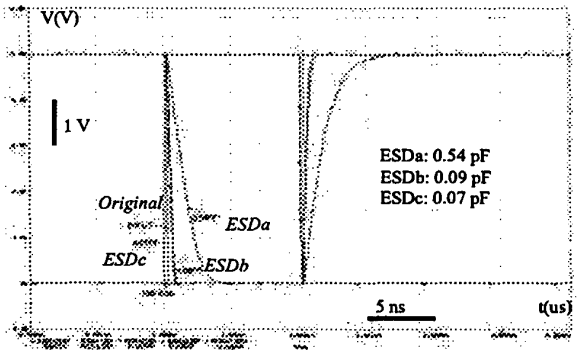

Fig. 7 In/Out waveforms of a ring oscillator with single C_{ESD} load showing clock corruption from ESDa and recovery in using advanced ESD b &c.

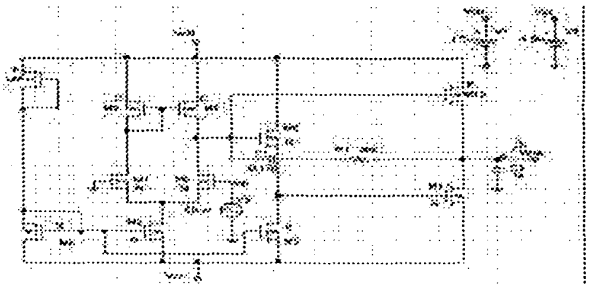

Fig. 8 Schematics of a low-power, high-speed Op Amp circuit.

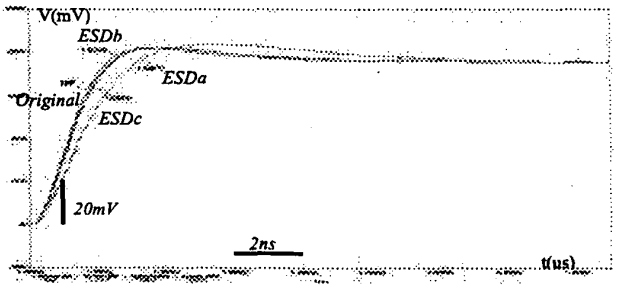

Fig. 9 Op Amp circuit: small-signal step response for settling time tests.